AMENDMENTS TO THE SPECIFICATION

Paragraph beginning at page 1, line 1 (before the Title):

~~DESCRIPTION~~

Please insert the following paragraph on page 1 after the title:

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is a national stage of PCT/JP2004/009319, filed July 1, 2004, which claims priority to Japanese application No. 2003-190488, filed July 2, 2003.

Paragraph beginning at page 1, line 3:

~~Technical~~ Field of the Invention

Paragraph beginning at page 1, line 10:

In ~~general~~ a first related art, a high-frequency oscillator device including an oscillation circuit for oscillating a signal having a predetermined oscillating frequency and a dielectric resonator, such as a TM010 mode resonator, for setting the oscillating frequency are disposed on a dielectric substrate is known for use in, for example, a communication device, (for example, see Patent Document 1).

Paragraph beginning at page 2, line 4:

In a ~~As the~~ second related art~~, the following oscillator device is known~~ (for example, see Non-Patent Document 1)~~. An~~, an oscillation circuit is formed on a substrate and a TE010 mode resonator is formed on another substrate, and the TE010 mode resonator is fixed on the substrate of the oscillation circuit. In the second related art, ~~the~~ an oscillator exhibiting excellent noise characteristics can be formed since the TE010 mode resonator has high Q (Quality factor) characteristics.

Paragraph beginning at page 4, line 3:

Summary ~~Disclosure~~ of the Invention

Paragraph beginning at page 9, line 14:

~~[Fig. 1]~~ Fig. 1 is a plan view illustrating an oscillator device according to a first embodiment of the present invention.

Paragraph beginning at page 9, line 17:

~~[Fig. 2]~~ Fig. 2 is an electric circuit diagram illustrating the oscillator device shown in Fig. 1.

Paragraph beginning at page 9, line 19:

~~[Fig. 3]~~ Fig. 3 is a perspective view illustrating a dielectric resonator chip and other components enlarged from those shown in Fig. 1.

Paragraph beginning at page 9, line 22:

~~[Fig. 4]~~ Fig. 4 is an exploded perspective view illustrating a dielectric resonator chip and other components enlarged from those shown in Fig. 1.

Paragraph beginning at page 9, line 25:

~~[Fig. 5]~~ Fig. 5 is an exploded plan view illustrating a dielectric resonator chip and other components enlarged from those shown in Fig. 1.

Paragraph beginning at page 10, line 3:

~~[Fig. 6]~~ Fig. 6 is an enlarged plan view illustrating the dielectric resonator chip only shown in Fig. 1.

Paragraph beginning at page 10, line 5:

~~[Fig. 7]~~ Fig. 7 is an enlarged bottom view illustrating the dielectric resonator chip only shown in Fig. 1.

Paragraph beginning at page 10, line 8:

~~[Fig. 8]~~ Fig. 8 is an exploded perspective view illustrating a computation model of, for example, a dielectric resonator chip.

Paragraph beginning at page 10, line 11:

~~[Fig. 9]~~ Fig. 9 is a sectional view illustrating the computation model of, for example, a dielectric resonator chip, taken along line IX-IX in Fig. 8.

Paragraph beginning at page 10, line 14:

~~[Fig. 10]~~ Fig. 10 is a characteristic diagram illustrating the relationship between the gap formed in the dielectric resonator chip shown in Fig. 9 and the resonant frequency and the electric energy concentration.

Paragraph beginning at page 10, line 18:

~~[Fig. 11]~~ Fig. 11 is a characteristic diagram illustrating the relationship between the frequency and the reflection loss caused by the dielectric resonator chip shown in Fig. 1.

Paragraph beginning at page 10, line 22:

~~[Fig. 12]~~ Fig. 12 is a characteristic diagram enlarged from the diagram having a frequency range from 37.5 GHz to 38.5 GHz in Fig. 11.

Paragraph beginning at page 10, line 25:

~~[Fig. 13]~~ Fig. 13 is an enlarged plan view illustrating a dielectric resonator chip according to a first modified example.

Paragraph beginning at page 11, line 3:

~~[Fig. 14]~~ Fig. 14 is an enlarged bottom view illustrating the dielectric resonator chip shown in Fig. 13.

Paragraph beginning at page 11, line 5:

~~[Fig. 15]~~ Fig. 15 is an enlarged plan view illustrating a dielectric resonator chip according to a second modified example.

Paragraph beginning at page 11, line 8:

~~[Fig. 16]~~ Fig. 16 is an enlarged bottom view illustrating the dielectric resonator chip shown in Fig. 15.

Paragraph beginning at page 11, line 10:

~~[Fig. 17]~~ Fig. 17 is a block diagram illustrating a communication device according to a second embodiment.

Paragraph beginning at page 12, line 7:

Detailed Description of ~~Best Mode for Carrying Out~~ the Invention